CLAIMS

What is claimed is:

1. A circuit for quantifying a high-voltage signal comprising:

a high-voltage input terminal having a first voltage;

an output terminal;

a field transistor having a drain, a gate, and a source, said gate connected to said high-voltage input terminal, said drain and source having a second voltage, said output terminal coupled to said drain;

wherein said output terminal provides a signal representative of said first voltage.

2. The circuit as defined in claim 1 wherein said field transistor further comprises:

a polysilicon gate; and

a gate oxide;

wherein said gate oxide is formed during a LOCOS step including a masked region masked by silicon-nitride, said gate oxide formed in a region absent of silicon-nitride.

3. The circuit of claim 2 wherein said gate oxide has a thickness of at least 0.1 micron.

4. The circuit of claim 2 wherein said gate oxide has a thickness of at least 0.5 micron.

5. The circuit of claim 1 wherein said field transistor comprises a metal gate layer deposited over a thermal oxide.

6. The circuit of claim 1 wherein said field transistor comprises a metal gate transistor in which the metal gate is formed over an active region and a

thick, oxide layer deposited as a pre-metal dielectric after poly deposition above the active region.

7. The circuit of claim 1 wherein said field transistor comprises a metal gate transistor in which the metal gate is formed over a deposited oxide which lies upon a LOCOS oxide.

8. The circuit as defined in claim 1 wherein said field transistor comprises a NMOS transistor

9. The circuit as defined in claim 1 wherein said field transistor comprises a PMOS transistor

10. The circuit as defined in claim 1 wherein said field transistor is formed over a n-type region.

11. The circuit as defined in claim 1 wherein said field transistor is formed over a p-type region.

12. The circuit as defined in claim 2 wherein said field transistor further includes a drain extension region formed under said gate oxide by a dopant species introduced before said LOCOS step in a region absent of said silicon-nitride.

13. The circuit as defined in claim 6 wherein said field transistor further includes a drain extension region formed under said active region by a dopant species implanted into said active region.

14. A circuit, comprising:

at least one low voltage input;

at least one high voltage terminal; and

a first field transistor having a source, a drain and a control region;

wherein said control region is coupled to said high voltage terminal.

15. The circuit of claim 14 wherein said circuit further includes a second field transistor coupled to said first field transistor.

16. The circuit of claim 15 wherein each field transistor includes a cascode transistor coupled thereto.

17. The circuit of claim 14 wherein said first field transistor comprises a NMOS transistor.

18. The circuit of claim 14 wherein said first field transistor comprises a PMOS transistor.

19. The circuit of claim 15 wherein each field transistor has a width, and wherein said second field transistor has a width which is greater than the width of the first field transistor.

20. The circuit of claim 19 wherein the width of the second field transistor is about 10 times greater than that of the first field transistor.

21. The circuit of claim 14 wherein said field transistor comprises a MOS transistor having an oxide separating said source and said drain regions and said control region, and said oxide has a thickness greater than the maximum thickness available to other devices on an integrated circuit chip on which the circuit is manufactured.

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22. The circuit of claim 21 wherein the field transistor is a NMOS transistor.

23. The circuit of claim 21 wherein the field transistor is a PMOS transistor.

24. The circuit of claim 21 wherein the oxide has a thickness of at least 1000 Angstroms.

25. The circuit of claim 14 further including a second field transistor, each field transistor having coupled thereto a cascode transistor and a mirror transistor, wherein each field transistor is coupled to a first rail and each mirror transistor is coupled to a second rail.

26. The circuit of claim 25 wherein each field transistor further comprises a width and a drain current, and the width of the second field transistor is greater than that of the first field transistor, such that a bias applied to the cascode transistors generates a gain between said drain currents dependent upon the ratio of the width of the second transistor to the first transistor.

27. The circuit of claim 25 wherein said high voltage terminal has a swing of at least 40 v.

28. The circuit of claim 25 wherein an input voltage has a swing of no greater than 15 v.

29. The circuit of claim 14 further including a second field transistor, each field transistor having coupled thereto a cascode transistor and a mirror transistor, wherein each field transistor is coupled to a first rail and each

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mirror transistor is coupled to a second rail and the gate of each cascode transistor is coupled to a cascode voltage.

30. The circuit of claim 29 wherein the mirror transistor coupled to the first field transistor is a diode connected input to a current mirror.

31. The circuit of claim 30 wherein the second field transistor is connected to a mirror output.

32. A high-voltage amplifier comprising

an input terminal;

a high-voltage output terminal;

a first field transistor having a gate a source and a drain;

a second field transistor having a gate a source and a drain;

an electrical connection between said high-voltage output terminal and said first field transistor gate; and

an electrical connection between said input terminal and said second field transistor gate

33. The amplifier of claim 32 further including a current-differencing circuit coupled to said first field transistor and said second transistor, said current-differencing circuit having an output.

34. The amplifier of claim 33 further including a trans-impedance stage having an input and an output, said trans-impedance stage input coupled to said current-differencing circuit output, .

35. The amplifier of claim 33 said current-differencing circuit further including:

a first input current;

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a second input current;

wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current.

36. The amplifier of claim 32 wherein the source of said second field transistor is operatively coupled to said source of said first field transistor, and said drain of said second field transistor is operatively coupled to said drain of said first field transistor.

37. The amplifier of claim 32 further including a first cascode transistor having a source connected to said drain of said first field transistor, and a second cascode transistor having a source connected to said drain of said second field transistor.

38. The amplifier of claim 32 wherein each transistor has a size including a length and a width, and the width of the first transistor is less than the width of the second transistor.

39. The amplifier of claim 38 wherein the width of the second transistor is at least 10 times greater than that of the first transistor.

40. The amplifier of claim 38 wherein the gain of the amplifier is dependent upon the ratio of the widths of the first and second transistors.

41. A differential high-voltage amplifier comprising:

a first high-voltage terminal;

a second high-voltage terminal;

a first field transistor having a gate a source and a drain, said first field transistor gate coupled to said first high-voltage terminal;

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a second field transistor having a gate a source and a drain said second field transistor gate coupled to said first high-voltage terminal; and

a third transistor having a gate a source and a drain, the gate of said third transistor comprising a first input terminal.

42. The amplifier of claim 41 wherein said third transistor further comprises a resistance, said resistance being responsive to a voltage applied to said first input terminal.

43. The amplifier of claim 41 further including fourth transistor having a gate, drain, and source, said gate comprising a second input terminal.

44. The amplifier of claim 43 further including a current-differencing circuit having at least one output.

45. The amplifier of claim 44 said current-differencing circuit further including:

a first input current; and

a second input current;

wherein said at least one output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current.

46. The amplifier of claim 41 further including a common-mode reference, a common-mode detector having an output, and a feedback connection.

47. The amplifier of claim 46 wherein said common-mode detector output is responsive to common mode voltage of said first and second high-voltage terminals, and said feedback connection is responsive to differences

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between said common-mode detector output and said common-mode reference.

48. The amplifier of claim 46 further including a fifth transistor, a sixth transistor, and a seventh transistor wherein said fifth through seventh transistors are field transistors having a gate, a drain, and a source, said gate of said fifth transistor connected to said first high-voltage terminal, said gate of said sixth transistor connected to said second high-voltage terminal, said seventh transistor gate connected to said common-mode reference.

49. The amplifier of claim 48 wherein said feedback connection further includes an input and an output, said drain of said fifth through seventh transistors being connected to said feedback connection input, said feedback connection output coupled to said first high-voltage output and said second high-voltage output.

50. An integrated circuit, comprising:

a high voltage output stage having a first terminal and a second terminal;

a common mode feedback circuit including a first field transistor and a second field transistor, each transistor having a control gate, said control gate of the first field transistor coupled to said first terminal and said control gate of said second field transistor coupled to said second terminal, respectively; and

a differential mode feedback circuit, including a differential input and a third field transistor and a fourth field transistor, each of said third and fourth transistors having a gate, the gate of said third field transistor coupled to said first terminal and said gate of said fourth transistor coupled to said second terminal.

51. The high voltage amplifier of claim 50 wherein said differential mode feedback circuit includes a differential current output coupled to said high voltage output stage.

52. The high voltage amplifier of claim 51 wherein said differential mode feedback circuit includes a current differencer.

53. The high voltage amplifier of claim 52 wherein the current differencer includes a current amplifier.

54. The high voltage amplifier of claim 50 wherein the common mode feedback circuit includes a common mode reference voltage, and the common mode feedback circuit is responsive to the common-mode voltage of the output stage.

55. A high-voltage amplifier comprising:

an input terminal;

a high-voltage output terminal;

a first field transistor having a gate a source and a drain;

an electrical connection between said high-voltage output terminal and said first field transistor gate;

a reference circuit;

a current-steering circuit having an input and an output.

56. The amplifier as described in claim 55 wherein said reference circuit further includes an output terminal, said current-steering circuit further includes a coupling from said input to said input terminal, wherein said current steering circuit is coupled to said reference circuit output terminal.

57. The amplifier as described in claim 56 wherein said reference circuit further includes a second field transistor having a gate and a reference voltage connected to said second field transistor gate.

58. The amplifier as described in claim 55 further including a differencing circuit having a first input, a second input, and an output, said first input coupled to said first field transistor and said second output coupled to the output of said current-steering circuit.

59. An optical mirror array, comprising:

at least one MEMS mirror having a high-voltage input;

a high voltage core having a first terminal and a second terminal, one or more of said first and second terminals coupled to said high-voltage input;

a common mode feedback circuit including a first field transistor and a second field transistor, each transistor having a control gate, the control gate of the first field transistor coupled to said first terminal and said control gate of said second field transistor coupled to said second terminal, respectively; and

a differential mode feedback circuit, including a differential input and a third field transistor and a fourth field transistor, each transistor having a gate, the gate of said third field transistor coupled to said first terminal and said gate of said fourth transistor coupled to said second terminal.

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